Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of operating an integrated circuit comprising:
providing a differential output driver at an output of the integrated circuit, wherein the differential output driver has a first slew rate mode and a second slew rate mode;
configuring the differential output driver to operate in the first or second slew rate mode;
when in the first slew rate mode, providing an input signal having a first edge rate to an input of the differential output driver; and
when in the second slew rate mode, providing an input signal having a second edge rate to the input of the differential output driver, wherein the second edge rate is slower than the first edge rate.

[c2] The method of claim 1 wherein when the differential output driver is in the second slew rate mode, the input signal driving the differential output driver has voltage swing of X volts, which is less than a voltage swing of the input signal when the differential output driver is in the first slew rate mode.

[c3] The method of claim 1 wherein the differential output driver comprises:

a first PMOS transistor coupled between a first supply line and a first output node of the differential output driver;
a first NMOS transistor coupled between the first output node and a second supply line;
a second PMOS transistor coupled between the first supply line and second output node of the differential output driver;
a second NMOS transistor coupled between the second output node and the second supply line; and
an impedance device coupled between the first and second output node.

[c4] The method of claim 3 wherein the input signal is coupled to gates of the first PMOS and first NMOS transistors, and an inverted input signal is coupled to gates of the second PMOS and second NMOS transistors.

[c5] The method of claim 4 wherein when the input signal has the second edge rate slower than the first edge rate, the inverted input signal has a third edge rate, slower than a fourth edge rate of the inverted input signal during the first slew rate mode.

[c6] The method of claim 1 wherein the differential output driver comprises a plurality of NMOS transistors, each of the plurality having a different number of legs and a

separate gate input, and the input signal is coupled to one of more of the separate gate inputs of the plurality of NMOS transistors.

[c7] The method of claim 1 wherein the integrated circuit is a programmable logic integrated circuit.

[c8] The method of claim 1 wherein configuring the differential output driver to operate in the first or second slew rate mode comprises programming an SRAM memory cell, EPROM memory cell, EEPROM memory cell, or Flash memory cell.

[c9] A method of operating an integrated circuit comprising:
providing a differential output driver at an output of the integrated circuit, wherein the differential output driver has a first slew rate mode and a second slew rate mode;
when in the first slew rate mode, driving an input of the differential output driver with a predriver outputting a signal from a first voltage level to a second voltage level; and
when in the second slew rate mode, driving the input of the differential output driver with the predriver outputting a signal from the first voltage level to a third voltage level, where the third voltage level is less than the second voltage level.

[c10] The method of claim 9 wherein when in the second slew rate mode, an input signal driving the differential output driver has an edge rate of X volts per second, which is less than an edge rate of the input signal when the differential output driver is in the first slew rate mode.

[c11] The method of claim 9 wherein a first difference between the second and first voltage levels is greater than a second difference between the third and first voltage levels.

[c12] The method of claim 9 wherein the integrated circuit is a programmable logic integrated circuit.

[c13] The method of claim 9 wherein the differential output driver comprises a plurality of NMOS transistors, each of the plurality having a different number of legs and a separate gate input, and the input of the differential output driver is coupled to one of more of the separate gate inputs of the plurality of NMOS transistors.

[c14] An integrated circuit comprising:
a differential output driver circuit comprising an output transistor comprising a first transistor group comprising a first on resistance and first control electrodes, a second transistor group comprising a second on resistance and second control electrodes, and a third transistor group comprising a third on resistance and third control

electrodes, wherein the first on resistance is less than the second on resistance, which is less than the third on resistance;

a first predriver coupled to the first control electrodes;

a second predriver coupled to the second control electrodes; and

a third predriver coupled to the third control electrodes, wherein at least one of the first, second, or third predriver is enabled to drive the differential output driver.

[c15] The integrated circuit of claim 14 wherein at least any two of the first, second, and third predrivers are enabled to drive the differential output driver.

[c16] The integrated circuit of claim 14 wherein the first, second, and third predrivers are enabled to drive the differential output driver.

[c17] The integrated circuit of claim 14 wherein the integrated circuit is a programmable logic integrated circuit.

[c18] An integrated circuit comprising:

a differential output driver circuit comprising an output transistor comprising a first transistor group comprising a first number of legs and first control electrodes, a second transistor group comprising a second number of

legs and second control electrodes, and a third transistor group comprising a third number of legs and third control electrodes, wherein the first number of legs is greater than the second number of legs, which is greater than the third number of legs;

a first predriver coupled to the first control electrodes;

a second predriver coupled to the second control electrodes; and

a third predriver coupled to the third control electrodes, wherein at least one of the first, second, or third predriver are enabled to drive the differential output driver.

[c19] The integrated circuit of claim 18 further comprising:

a control circuit to enable at least one of the first, second, or third predriver based on a configuration of plurality of slew rate control bits.

[c20] The integrated circuit of claim 18 wherein the first predriver provides a output signal to the first control electrodes having a first edge rate or a second edge rate, wherein the first edge rate is faster than the second edge rate.